Department Of Computer Application (BCA)
Dr. Rakesh Ranjan

BCA Sem - 2
Computer Organization and Architecture

FLIP-FL0P CIRCUIT :-

Flip Flop is a sequential electronic circuit that is used to store 1 bit information i.e 0 and 1. Sequential electronic circuit produces the output on the basis pr present input as well as the previous output of the circuit. To store the information in flipflop, two state, set and reset are used along with clock signal. The set state represent the value 1 and the reset state represent the value 0. All flipflop generate two output- one is present output and other is complemented value of output.

Followings are important flip-flop

1. SR Flip-flop
2. D-flipflop
3. JK flipflop
4. T-type flipflop

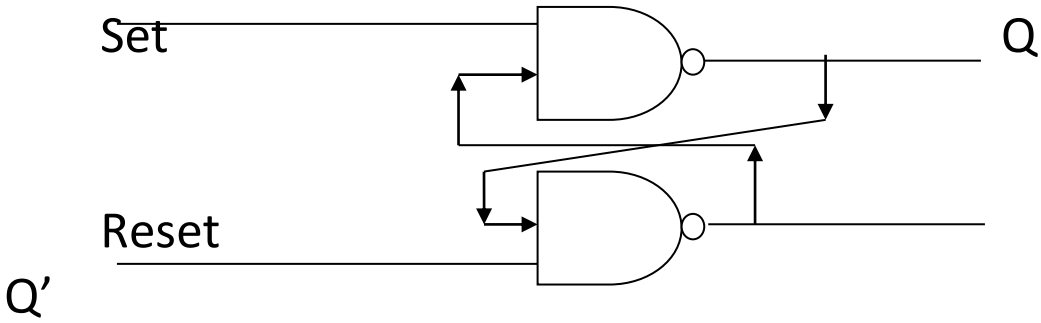
1. SR Flip-flop-> this flip flop consist of two NAND gate which accept two input. One output is externally provided to each the NAND gate while the other input is provided by connecting the previous output of NAND Gate.

   The truth table of SR Flip flop may be shown as :-

Input	Output

Set	Reset	Q	Q’
0	0	Qn-1	Qn-1’
0	1	0	1
1	0	1	0
1	1	Unstable state	

The circuit may be shown as:

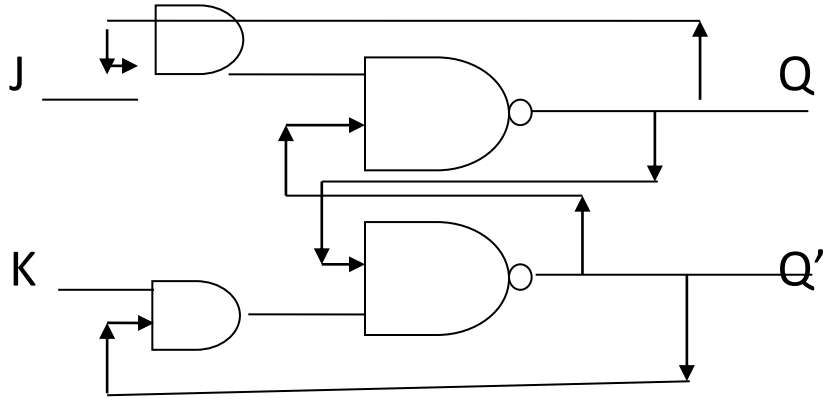


2. J.K Flip Flop :- the disadvantage of SR flip flop is that the output is undefined when both the input to set 1. This situation is called race condition. JK flip flop is advancement over SR flip flop. It eliminates the race condition flip is reencountered in SR Flip-Flop

   The truth table of J.K flip flop :

Input		Output	
J	k	Q	Q’
0	0	Qn-1	Qn-1’
0	1	0	1
1	0	1	0
1	1	Qn-1’	Qn-1

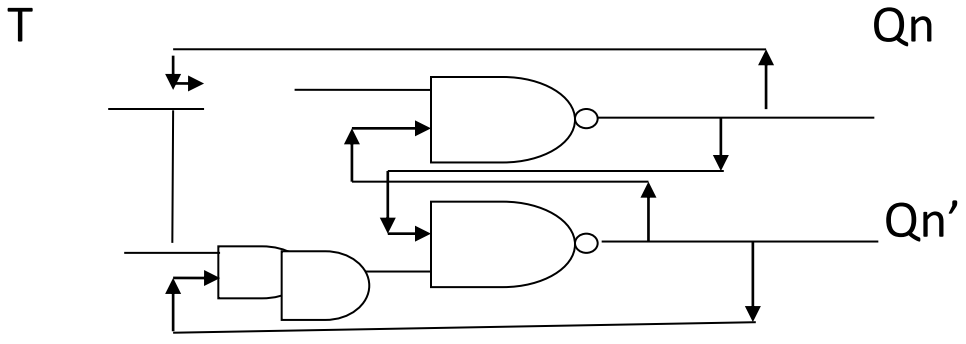
The circuit may be shown as



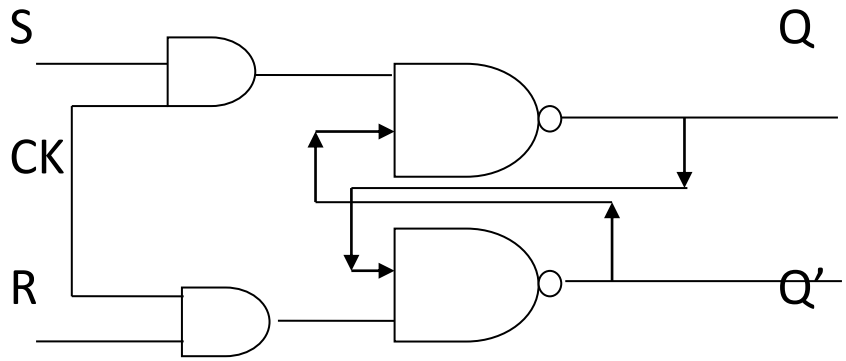
3. T- Flip Flop- T Flip-flop type is an enhanced version of the jk flip flop that accepts one input. Here, same input is applied in both the AND gate of jk flip flop. The truth table of T- Flip flop as :-

Input	Output
T	Qn
0	Qn
1	Qn'

The circuit may be shown as :-



Clocked SR Flip Flop :- clocked SR flip Flop is built with a clock pulse to control the output of the SR Flip flop circuit. If the clock pulse (CK=1) its operation is exactly the same as SR flip flop. On the other hand when the clock pulse is not present (CK=0) the first gate are initiated i.e their output are 1 irrespective of the value of S and R. it means , the circuit responds to the input S and R only when clock pulse is available



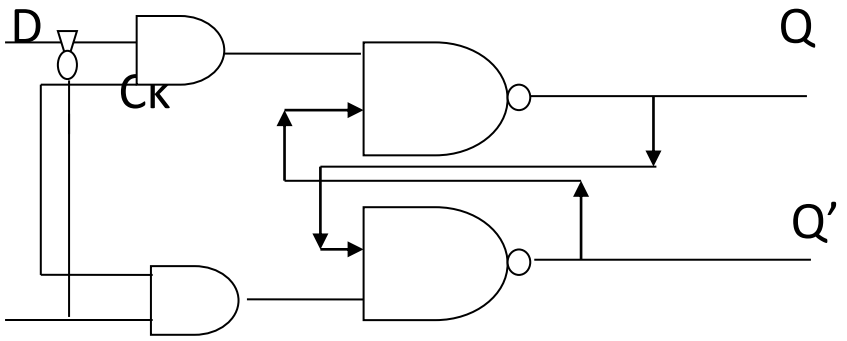
D flip Flop :- D flip flop is the enhanced version of Clocked SR flip flop. In SR Flip flop two input S and R are connected to an AND gate along with clock input. The output of each AND gate then applied to the NAND gate . The inclusion of clock signal ensure that the flip flop can be set or reset only when clock pulse is provided to the circuit.

In D-flip flop the same input is directly applied to the first and gate and a complemented of S is applied to second NAND gate . as a result the circuit will output as the input signal .

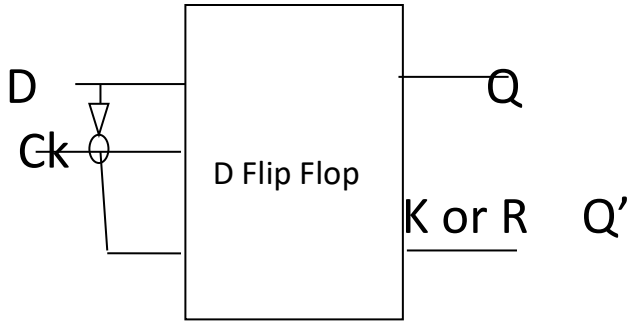
The truth table may be shown as :

Input	Output
D	Q
0	0
1	1

The circuit may be shown as



J or S



----------x----------